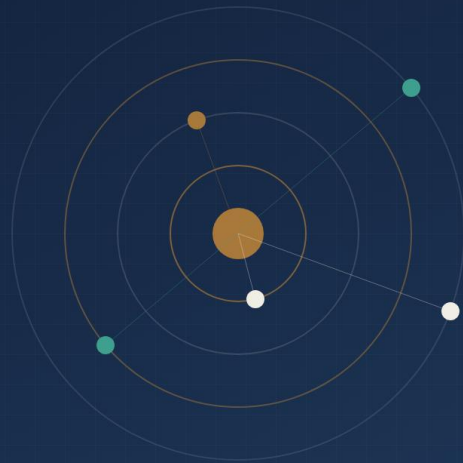


Gonagoor
Angel Network

Incubating deep technology, hands-on



Case study

From silicon idea to sovereign compute

How Gonagoor Technology Solutions incubated Sudarshana Semiconductors through six layers of hands-on support

Prepared by

Gonagoor Technology Solutions

A select circle of technologically inclined angels backing the next wave of deep technology

Angel Investor: Prashanth Raghu

Abstract

The core argument

Chip startups rarely fail because the architecture is weak. They fail because silicon is unforgiving: one flawed assumption, one missed tape-out or one unfunded quarter can end the programme. Incubation closes that gap by supplying leadership, rigour, verification, funding and market access together, before the first design is committed to a foundry.

Sudarshana Semiconductors is a Bengaluru-based chip design venture building original processor architectures for AI inference and high-performance parallel computing. Its aim is to move Indian semiconductor work from designing chips for others towards sovereign compute platforms, with intelligence accelerated in the hardware itself.

Few areas of deep technology are as demanding. Design cycles run for years, tools and talent are scarce, and a respin after fabrication costs far more than any early-stage budget can absorb. A founder team strong in architecture still needs seasoned leadership, deep verification, funding beyond equity and a credible route to design wins.

Gonagoor responded with a structured incubation programme. Angels did not act as passive investors. Each took a working role as technology leader and mentor, and capital was deployed gradually, at an average of Rs. 1.5 lakh a month over the first year, so that funding followed real milestones. This case study documents six layers of that support and what each one gives a chip venture.

Why incubation, not just capital

- **Capability gap.** Founders need a CEO, CTO and marketing head on day one and can afford none of them full time.
- **Time gap.** Deep-tech milestones are measured in years, while a cheque runs out in months. Support must stretch the runway and de-risk each stage.
- **Readiness gap.** Investors back proof and preparation. Ventures that arrive without either are passed over, however good the science.

At a glance

Item	Detail
Venture	Sudarshana Semiconductors Private Limited
Location	Bengaluru
Sector and technology	Semiconductor and VLSI: original processor architectures for AI inference and high-performance parallel computing
Also co-incubated with	IIT Madras Incubation Cell (2025), IIM Lucknow EIC
Stage at entry	TRL 2
Network framework	Capital of Rs. 45 lakh

Item	Detail
Angel role	Fractional Technology leader and mentor, working inside the venture

1. Fractional CEO, CTO and marketing support



The need

A chip venture needs experienced leadership on three fronts at once: a chief executive who can raise capital and win foundry and IP partners, a technical head who has taken silicon to tape-out, and a marketer who can position an unproven architecture against global incumbents. Few early teams can afford all three, and chip design talent is scarce and expensive to hire.

What Gonagoor provided

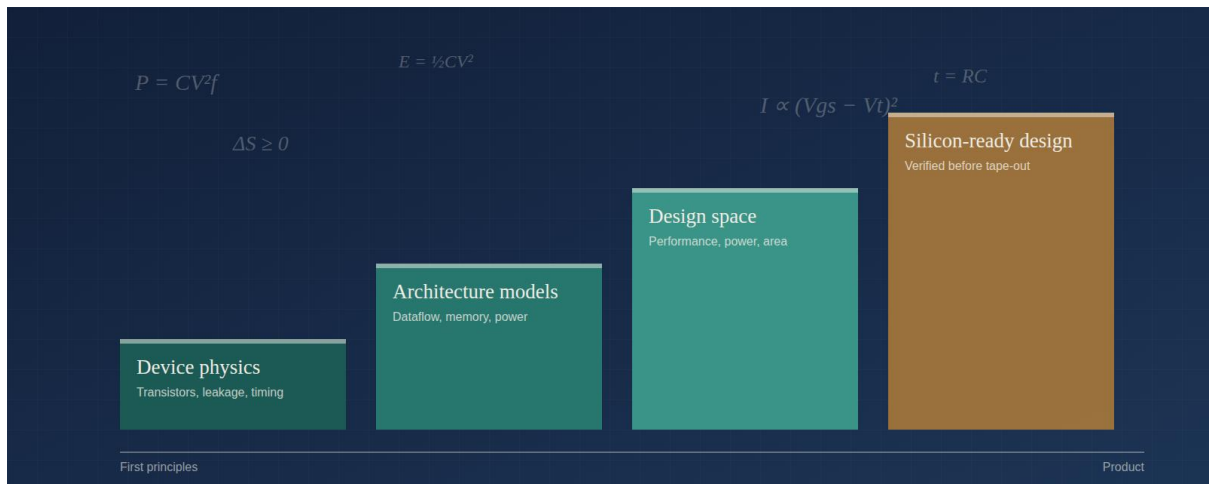
- **Fractional CEO.** Guides hiring of scarce design talent, shapes partnerships with foundries and IP vendors, and leads the financing plan and investor story.
- **Fractional CTO.** Reviews the architecture and design flow, sets tape-out milestones and keeps engineering choices tied to workloads customers will pay for.
- **Fractional marketing lead.** Frames the sovereign-compute thesis, defines the target workloads and turns architectural advantages into a message buyers can act on.

Value to Sudarshana Semiconductors

Sudarshana gains a senior leadership bench for a fraction of the cost. Its founders stay focused on architecture while experienced hands run the company and the programme around them.

Outcome to record: 120pc reduction of costs compared to a full time CxO team.

2. First-principles development support



The need

Many processor designs start from familiar templates. For AI inference that is risky, because performance is set by memory movement, energy per operation and data reuse rather than by raw arithmetic. A design built on borrowed assumptions can look strong on paper and disappoint in silicon. Based on the hyperspectral physics framework, developed by Gonagoor technologies, Sudarshana rapidly iterated to hallucination free inference designs in GPUs and FPGA hardware.

What Gonagoor provides

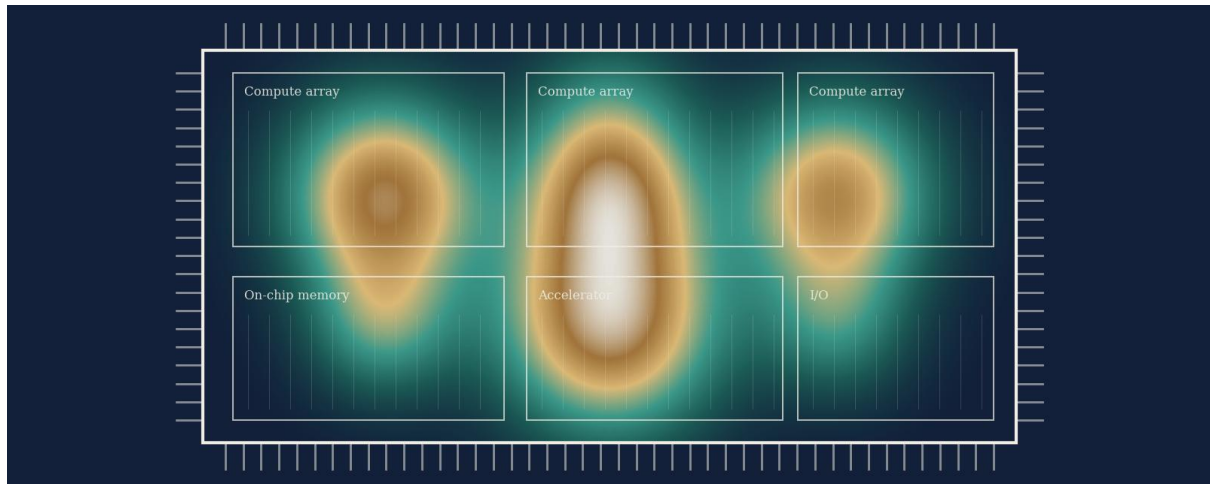
- **Research-led foundations.** Gonagoor's research work is the starting point, so Sudarshana builds on established fundamentals rather than repeating them.
- **Architecture from the workload.** Design choices are derived from the physics of data movement, power and timing, and from the behaviour of the target models.
- **Limits and trade-offs.** The team maps performance, power and area limits early, so effort goes where the gains are real.

Value to Sudarshana Semiconductors

Sudarshana's architecture rests on understanding rather than imitation. That lowers technical risk, sharpens the case against incumbents and produces intellectual property that is defensible.

Outcome to record: 350pc reduced time of development of design.

3. Support for world-class simulations



The need

After fabrication, mistakes are almost impossible to fix. Chip teams therefore live or die by pre-silicon verification: architectural simulation, RTL simulation, power and thermal analysis and hardware emulation. This needs skill and tooling that a young venture does not have. Based on the Gonagoor hardware design verification framework, Sudarshana's designs ensured they failed more on software than on the real tapeout.

What Gonagoor provides

- **Architectural simulation.** Explores dataflow, memory hierarchy and scheduling choices against real AI workloads before any RTL is written.
- **Power, timing and thermal analysis.** Checks that a design meets its targets and finds hot spots and bottlenecks early.
- **Prototype and emulation.** Uses FPGA prototyping and emulation to run software on the design, so bugs surface before tape-out.

Value to Sudarshana Semiconductors

Sudarshana finds errors on a screen instead of on a wafer. Fewer respins, faster learning and credible performance evidence for customers and investors follow.

Outcome to record: 600pc reduced need for failed tapeouts.

4. Grant support



The need

Chip design is capital heavy, and India now has several programmes that fund design work, tools and fabrication access without taking equity. The schemes are many, the applications are demanding and the windows are short. Small teams miss them or apply with proposals that do not match what reviewers score.

What Gonagoor provides

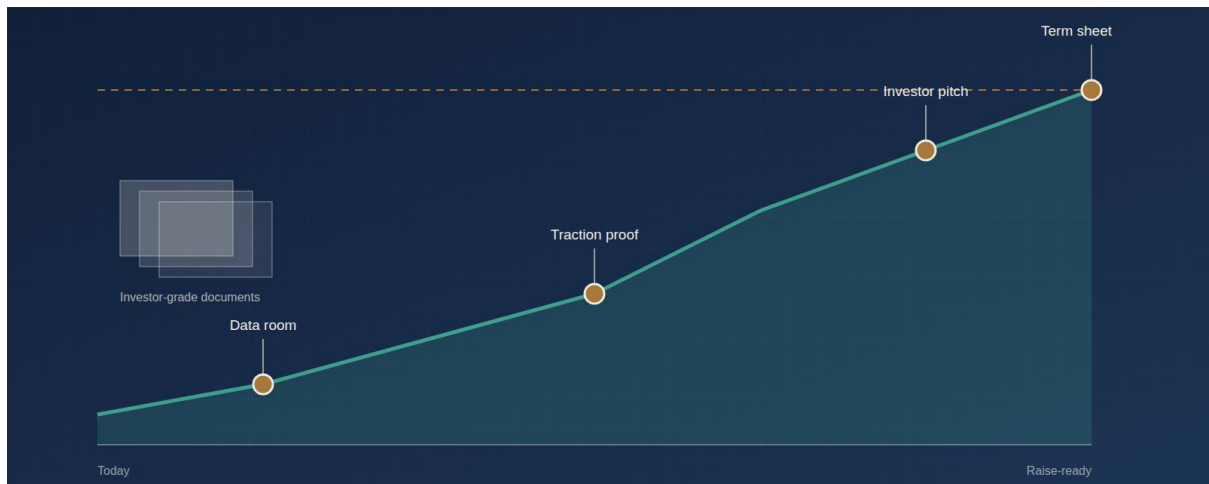
- **Opportunity mapping.** Identifies fitting programmes, such as the design-linked incentive and chip-design support schemes under the India Semiconductor Mission and related MeitY initiatives, and confirms current terms.
- **Proposal craft.** Angels with technical depth help frame the architecture, the innovation and the milestones so the case is clear to reviewers.
- **Access to tools and fabrication.** Helps the team use shared design infrastructure and multi-project wafer runs to cut the cost of early silicon.

Value to Sudarshana Semiconductors

Non-dilutive funding extends Sudarshana's runway and keeps more ownership with the founders. An award also acts as an independent stamp of technical merit.

Outcome to record: 7.5 lakhs of grant raised from CSR grants.

5. Funding preparedness



The need

Chip investors ask hard questions early: who owns the intellectual property, what does the path to tape-out cost, what does each milestone prove and what happens if a respin is needed. Ventures that arrive without clear answers lose momentum, and sometimes the round.

What Gonagoor provides

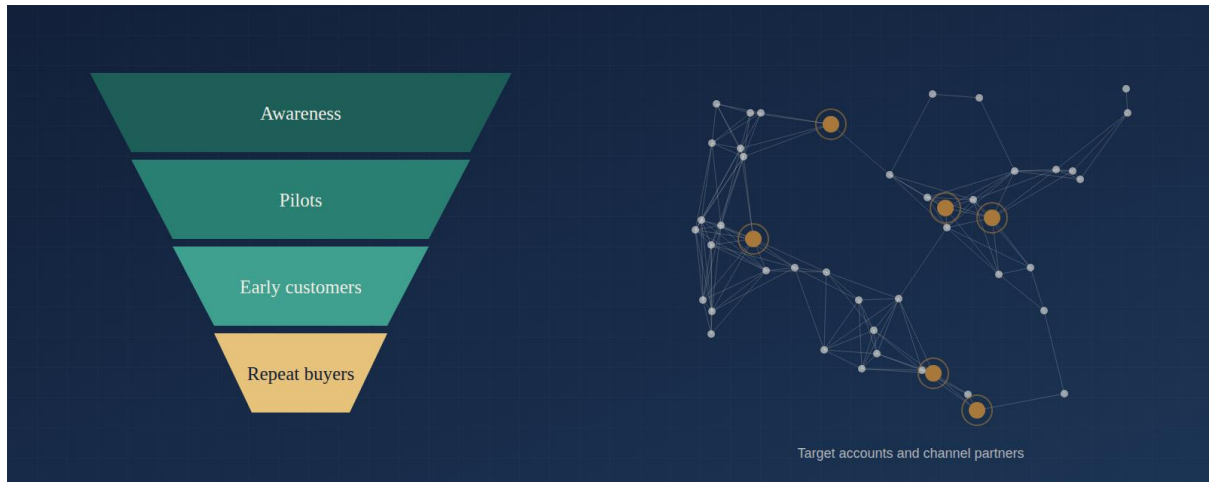
- **Data room.** Builds an organised diligence folder covering architecture, IP ownership, licences, legal and financial records.
- **Milestone-based financial plan.** Ties the raise to tape-out gates, tools, talent and fabrication costs, with runway and use of funds made explicit.
- **Pitch and introductions.** Sharpens the narrative through rehearsal and opens doors to investors who understand semiconductor timelines.

Value to Sudarshana Semiconductors

Sudarshana reaches investors ready for diligence, with a staged plan that shows how each rupee reduces technical risk.

Outcome to record: 120 VCs approached to and pitched.

6. Go-to-market support



The need

A new processor architecture sells to cautious buyers who must rewrite software and redesign boards to adopt it. Design wins are slow and depend on trust, tooling and proof. Without a deliberate route to market, strong silicon stalls at the evaluation stage.

What Gonagoor provides

- **Target workloads and customers.** Focuses on the AI inference and high-performance workloads where the architecture has a clear advantage, and on buyers who value sovereign compute.
- **Evaluation to design win.** Structures early-access programmes, reference designs and software kits so trials convert into commitments.
- **Partners and channels.** Uses the network's contacts to reach system makers, cloud and edge operators and public-sector buyers.

Value to Sudarshana Semiconductors

Sudarshana moves from working silicon to design wins with a plan, not by chance. Early customers and references then strengthen every later fundraise.

Outcome to record: ISRO, IIT Guwahati successfully run paid pilot deployments.

Summary and way forward

The six layers of support work as one system. Leadership keeps the venture organised, first-principles work and simulation make the architecture sound before silicon is committed, grants stretch the runway, funding preparedness earns investor confidence and go-to-market turns silicon into design wins.

Support layer	Risk it removes
Fractional CEO, CTO, marketing	Leadership gaps and poor early decisions
First-principles development	Flawed architecture assumptions
World-class simulation	Costly respins after fabrication
Grant support	Early cash pressure and dilution
Funding preparedness	Failed or weak fundraises
Go-to-market	Stalled evaluations and no design wins

The model in one line

Angels who are technologists invest capital and time together. That combination is what lets a young venture grow into a company that creates lasting value.